EXHIBIT A

Posted 10-6-07

021202-000900US

GTG. WC/Tras

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046301-046000

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,530	12/12/2001	Robert T. Plunkett	021202-000900US	7763

20350 7590 01/10/2007

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

MAIL DATE	DELIVERY MODE
01/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

Notice of Abandonment

Application No.	Applicant(s)	
10/015,530	PLUNKETT ET AL.	
Examiner	**Art Unit**	
Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

This application is abandoned in view of:

1. ☒ Applicant's failure to timely file a proper reply to the Office letter mailed on *09 December 2005*.
   (a) ☐ A reply was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply (including a total extension of time of _____ month(s)) which expired on _____.
   (b) ☐ A proposed reply was received on _____, but it does not constitute a proper reply under 37 CFR 1.113 (a) to the final rejection.
   (A proper reply under 37 CFR 1.113 to a final rejection consists only of: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114).
   (c) ☐ A reply was received on _____ but it does not constitute a proper reply, or a bona fide attempt at a proper reply, to the non-final rejection. See 37 CFR 1.85(a) and 1.111. (See explanation in box 7 below).
   (d) ☒ No reply has been received.

2. ☐ Applicant's failure to timely pay the required issue fee and publication fee, if applicable, within the statutory period of three months from the mailing date of the Notice of Allowance (PTOL-85).
   (a) ☐ The issue fee and publication fee, if applicable, was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the statutory period for payment of the issue fee (and publication fee) set in the Notice of Allowance (PTOL-85).
   (b) ☐ The submitted fee of $_____ is insufficient. A balance of $_____ is due.
   The issue fee required by 37 CFR 1.18 is $_____. The publication fee, if required by 37 CFR 1.18(d), is $_____.
   (c) ☐ The issue fee and publication fee, if applicable, has not been received.

3. ☐ Applicant's failure to timely file corrected drawings as required by, and within the three-month period set in, the Notice of Allowability (PTO-37).
   (a) ☐ Proposed corrected drawings were received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply.
   (b) ☐ No corrected drawings have been received.

4. ☐ The letter of express abandonment which is signed by the attorney or agent of record, the assignee of the entire interest, or all of the applicants.

5. ☐ The letter of express abandonment which is signed by an attorney or agent (acting in a representative capacity under 37 CFR 1.34(a)) upon the filing of a continuing application.

6. ☐ The decision by the Board of Patent Appeals and Interference rendered on _____ and because the period for seeking court review of the decision has expired and there are no allowed claims.

7. ☒ The reason(s) below:

See Continuation Sheet

Aimee J. Li
1/8/2007

Petitions to revive under 37 CFR 1.137(a) or (b), or requests to withdraw the holding of abandonment under 37 CFR 1.181, should be promptly filed to minimize any negative effects on patent term.

Item 7 - Other reasons for holding abandonment: Applicant's filed a Notice of Appeal on 09 May 2006 after paying a 2 month Extension of Time on 09 May 2006. No Appeal Brief or other reply has been received. The time period for the Notice of Appeal with all extensions of up to five months expired on 09 December 2006. The Examiner contacted Mr. C. Burt Sullivan (Reg. No. 41,516) on 05 January 2007 to confirm abandonment. Mr. Sullivan confirmed that no reply was sent by Townsend & Townsend and indicated that the case had been transferred to another attorney and suggested the Examiner contact Mr. Gerald Gray (Reg. No. 41,797), who would have the contact information of the new attorney. Both Mr. Sullivan and Mr. Gray provided contact information for Ms. Nancy Gamburd (Reg. No. 38,147). Ms. Gamburd contacted the Examiner on 08 January 2007 confirming that no reply was sent.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	10/015,530
Applicants	:	Paul L. Master *et al.*
Filed	:	December 12, 2001
Title	:	METHOD AND SYSTEM FOR MANAGING HARDWARE RESOURCES TO IMPLEMENT SYSTEM FUNCTIONS USING AN ADAPTIVE COMPUTING ARCHITECTURE
TC/A.U.	:	2183
Examiner	:	Aimee Li
Docket No.	:	046301-046000(QST046)
Customer No.	:	22204

DECLARATION OF MARC KAUFMAN

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I, Marc Kaufman, declare that I am a lawful age and if called upon to testify, I could and would competently testify to the facts set forth herein, namely:

1. I am a partner in the law firm of Nixon Peabody LLP and a registered patent attorney (Reg. No. 35,212). I was responsible for intake of the above-identified application file which was transferred by the assignee to my law firm on or about March 22, 2007.

2. The assignee notified me of discovery that the above-identified application was abandoned.

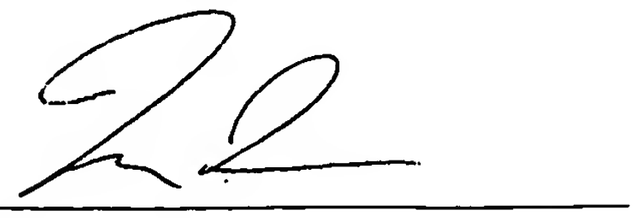
3. I and members of my firm promptly investigated the facts with the assignee and their representatives and prior counsels, in order to determine whether the attached Petition could be filed.

4. Based on the facts gathered, I determined to the best of my knowledge and belief that the attached Petition could be filed.

5. I declare that any delay was unintentional from the time the file was transferred to my law firm and I learned of the abandonment to the filing of the attached Petition.

I declare under the penalties of perjury that the foregoing are true and correct to the best of my knowledge and belief.

11-19-87
Date



Marc Kaufman

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	10/015,530
Applicants	:	Paul L. Master *et al.*
Filed	:	December 12, 2001
Title	:	METHOD AND SYSTEM FOR MANAGING HARDWARE RESOURCES TO IMPLEMENT SYSTEM FUNCTIONS USING AN ADAPTIVE COMPUTING ARCHITECTURE
TC/A.U.	:	2183
Examiner	:	Aimee Li
Docket No.	:	046301-046000(QST046)
Customer No.	:	22204

DECLARATION OF NANCY R. GAMBURD

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I, Nancy R. Gamburd, declare that I am a lawful age and if called upon to testify, I could and would competently testify to the facts set forth herein, as follows:

1. I am the managing member of the law firm Gamburd Law Group LLC and a registered patent attorney, USPTO Registration No. 38,147.

2. I was informed on or about late May or early June, 2006, by a consultant for the assignee of the above-identified application, that the file was to be transferred to my law firm from the patent counsel of record, Townsend, Townsend and Crew LLC ("Townsend"), as part of the transfer of more than 100 applications from various law firms representing the assignee.

3. The above-identified application file was transferred to my law firm from Townsend, on or about June 14, 2006. Although the transfer letter accompanying this file and approximately 30 other files from Townsend did contain notifications of upcoming due dates for *other* transferred applications, it did not contain any notification that a notice of appeal had been filed and that any Appeal Brief would be due within the next few weeks, on July 9, 2006, for the above-identified patent application.

4. I reviewed every file that was transferred to the Gamburd Law Group LLC for the purpose of making sure that all outstanding matters had been docketed and placed in my calendar, and did not notice a submission of a Notice of Appeal in the above-identified application file.

5. I was informed of the status of the application by the Examiner on or about January 8, 2007. After discussion, she indicated she would check with her Supervisor and determine whether an extension could be granted to avoid an abandonment. After the telephone call with the Examiner, I reexamined the file, and did find a Notice of Appeal among other loose papers which were not in any chronological order. I was subsequently informed in a second telephone call that the patent office could not grant any extension, and that a Notice of Abandonment would be mailed.

6. Any abandonment of the above-identified application due to a failure to file an Appeal Brief, following a Notice Of Appeal dated May 9, 2006 filed by the Townsend firm, was inadvertent and unintentional.

7. I was informed in March, 2007 that the above-identified application was to be transferred to new counsel at the law firm Nixon Peabody LLP.

8. I declare that any delay in filing a Petition to Revive the above-identified application was unintentional from the time the file was transferred to my law firm and I learned of the abandonment to the time the file was transferred from my law firm to the new counsel.

I declare under the penalties of perjury that the foregoing are true and correct to the best of my knowledge and belief.

November 16, 2007
Date

Nancy R. Gamburd

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	10/015,530
Applicants	:	Paul L. Master *et al.*
Filed	:	December 12, 2001
Title	:	METHOD AND SYSTEM FOR MANAGING HARDWARE RESOURCES TO IMPLEMENT SYSTEM FUNCTIONS USING AN ADAPTIVE COMPUTING ARCHITECTURE
TC/A.U.	:	2183
Examiner	:	Aimee Li
Docket No.	:	046301-046000(QST046)
Customer No.	:	22204

DECLARATION OF GERALD T. GRAY

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I, Gerald T. Gray, declare that I am a lawful age and if called upon to testify, I could and would competently testify to the facts set forth herein, namely:

1. I am a partner with the law firm of Townsend and Townsend and Crew LLP and a registered patent attorney, No. 41,797. Our firm was responsible for filing the above-identified application on December 12, 2001 on behalf of the applicants.

2. We were instructed by the assignee to file a Notice of Appeal in 2006. We proceeded to file a Notice of Appeal in response to a December 9, 2005 Final Office Action on May 9, 2006. We were informed by the assignee that they intended to proceed with appeal.

3. I was informed on or about June 8, 2006 that the above-identified application file was to be transferred to new counsel at the law firm, Gamburd Law Group LLC.

4. The above-identified application file was transferred to new counsel, Gamburd Law Group LLC, on or about June 14, 2006.

5. At the time the application file was transferred, our firm had not filed an Appeal Brief following the May 9, 2006 Notice of Appeal.

6. To the best of my knowledge and belief, at no time did the applicants or the assignee authorize myself or anyone in my firm to let the application go abandoned.

I declare under the penalties of perjury that the foregoing are true and correct to the best of my knowledge and belief.

11/9/07
Date

Gerald T. Gray

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application No.	:	10/015,530
Applicants	:	Paul L. Master *et al.*
Filed	:	December 12, 2001
Title	:	METHOD AND SYSTEM FOR MANAGING HARDWARE RESOURCES TO IMPLEMENT SYSTEM FUNCTIONS USING AN ADAPTIVE COMPUTING ARCHITECTURE
TC/A.U.	:	2183
Examiner	:	Aimee Li
Docket No.	:	046301-046000(QST046)
Customer No.	:	22204

CERTIFICATE OF EXPRESS MAILING
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I hereby certify that this paper is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 C.F.R. 1.10 to MS Appeal Brief Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on December 20, 2007.

Signature: Joanna Pinos

Joanna Pinos

Commissioner for Patents
Mail Stop Appeal Brief - Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF PURSUANT TO 37 C.F.R. § 41.37

Dear Sir:

This Appeal Brief is filed pursuant to the Appellants' appeal to the Board of Patent Appeals and Interferences ("Board") from the final rejection of claims 1-25 in a December 9, 2005 Final Office Action (Exhibit B). A Notice of Appeal was filed May 9, 2006 (*see* Exhibit C). This Appeal Brief is being filed with a petition for revival of this application for unintentional abandonment under 37 C.F.R. 1.137(b).

This Appeal Brief is being filed pursuant to 37 C.F.R. 1.137(b)(1) as the responsive paper to the December 9, 2005 Final Office Action.

I. REAL PARTY IN INTEREST

The real party in interest is QST Holdings LLC, having a place of business at 6640 Via Del Oro, Suite 120, San Jose, California 95119.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board of Patent Appeals and Interferences in the present appeal.

III. STATUS OF CLAIMS

Claims 1-25 are currently pending and rejected in the above-referenced application and are the subject of the present appeal. No claims have been allowed.

IV. STATUS OF AMENDMENTS

An Amendment and Response to Office Action was submitted on September 19, 2005 in reply to a July 14, 2004 Office Action. The pending claims are recent as of the September 19, 2005 Amendment.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claims 1, 6, 11, 16 and 21 are directed to the embodiments shown in Figs. 1, 3-4 and 11-14. Independent claim 1 is generally directed to an adaptive computing integrated circuit 100 configurable to perform a plurality of functions. (Exhibit A, Specification, p. 7, ¶ 29, Figs. 1, 3 and 4). The adaptable device 100 has a plurality of heterogeneous computational elements 250. (Ex. A, p. 10, ¶ 37). An interconnection network 110 (including networks 210, 240 and 220 in Figs. 3-4) is coupled to the plurality of heterogeneous computational elements 250 and the heterogeneous computational elements 250 are configurable by the network 210 in response to adaptation information. (Ex. A, p. 8, ¶ 33, p. 11, ¶ 39). A first group of heterogeneous computational elements is configurable to form a first functional unit to implement a first function. (Ex. A, p. 21, ¶ 67). A second group of heterogeneous computational elements is configurable to form a second functional unit to implement a second function. (Ex. A, p. 21, ¶ 67). If the second function is not currently used, one or more of the second group of heterogeneous computational elements are reconfigurable by forming one or more additional instances of the first functional unit. (Ex. A, p. 22, ¶ 71, Fig. 11).

Independent Claim 6 relates generally to an adaptive computing integrated circuit 100. (Ex. A, p. 7, ¶ 29, Figs. 1, 3 and 4). The adaptive computing integrated circuit 100 has a plurality of reconfigurable matrices 150. (Ex. A, p. 7, ¶ 29, Figs. 1, 3 and 4). The plurality of reconfigurable matrices 150 include a plurality of heterogeneous computational units 200. (Specification, pp. 9-10, ¶ 35, Figs. 1, 3 and 4). Each heterogeneous computational unit 200 has a plurality of fixed computational elements 250. (Specification, pp. 9-10, ¶ 35, Figs. 1, 3 and 4). The plurality of fixed computational elements 250 include a first computational element having a first architecture such as a multiplier 190 and a second computational element having a second

architecture such as an adder 195. (Ex. A, pp. 9-10, ¶¶ 38-39, Fig. 3). The plurality of the heterogeneous computational units 200 are coupled to an interconnect network 110 and reconfigurable in response to configuration information. (Ex. A, pp. 8-9, ¶ 33, p. 11, ¶ 39). A matrix interconnection network 110 is coupled to the plurality of reconfigurable matrices 150. (Specification, pp. 8-9, ¶ 33). The matrix interconnection network 110 is operative to reconfigure the plurality of reconfigurable matrices 150 in response to the configuration information for a plurality of operating modes. (Ex. A, pp. 8-9, ¶ 33, pp. 9-10, ¶ 35). A first group of heterogeneous computational units is reconfigurable to form a first functional unit to implement a first operating mode. (Ex. A, p. 21, ¶ 67). A second group of heterogeneous computational units is reconfigurable to form a second functional unit to implement a second operating mode. (Ex. A, p. 21, ¶ 67). If the second operating mode is not currently used, one or more of the second group of heterogeneous computational units are reconfigurable to implement the first operating mode. (Ex. A, p. 22, ¶ 71, Fig. 11).

Independent claim 11 relates generally to an adaptive computing integrated circuit 100. (Ex. A, p. 7, ¶ 29, Figs. 1, 3 and 4). The adaptive computing integrated circuit 100 has a plurality of heterogeneous computational elements 250. (Ex. A, p. 10, ¶ 37). The plurality of heterogeneous computational elements 250 includes a first computational element and a second computational element. (Ex. A, pp. 9-10, ¶¶ 38-39, Fig. 3). The first computational element has a first fixed architecture of a plurality of fixed architectures and the second computational element has a second fixed architecture of the plurality of fixed architectures and the first fixed architecture is different than the second fixed architecture. (Ex. A, pp. 10-11, ¶¶ 38-39, Fig. 3). The plurality of fixed architectures includes functions for memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and

field programmability. (Ex. A, p. 11, ¶ 39, p. 16, ¶ 49, Fig. 3). An interconnection network 110 is coupled to the plurality of heterogeneous computational elements 250 and the interconnection network 110 is operative to configure the plurality of heterogeneous computational elements 250. (Ex. A, p. 8, ¶ 33, p. 11, ¶ 39). A first group of heterogeneous computational elements is reconfigurable to form a first functional unit to implement a first function. (Ex. A, p. 21, ¶ 67). A second group of heterogeneous computational elements is reconfigurable to form a second functional unit to implement a second function. (Ex. A, p. 21, ¶ 67). If the second function is not currently used, one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network 110 to implement the first function. (Ex. A, p. 22, ¶ 71, Fig. 11).

Independent claim 16 generally relates to an adaptive computing integrated circuit 100. (Ex. A, p. 7, ¶ 29, Figs. 1, 3 and 4). The adaptive computing integrated circuit 100 includes a plurality of heterogeneous computational elements 250. (Ex. A, p. 10, ¶ 37). The plurality of heterogeneous computational elements 250 includes a first computational element and a second computational element. (Ex. A, pp. 10-11, ¶¶ 38-39, Fig. 3). The first computational element has a first fixed architecture and the second computational element has a second fixed architecture. (Ex. A, pp. 10-11, ¶¶ 38-39, Fig. 3). The first fixed architecture is different than the second fixed architecture. (Ex. A, pp. 10-11, ¶¶ 38-39, Fig. 3). An interconnection network 110 is coupled to the plurality of heterogeneous computational elements 250. (Ex. A, p. 8, ¶ 33, p. 11, ¶ 39). The interconnection network 110 is operative to configure a first group of heterogeneous computational elements 250 to form a first functional unit for a first functional mode of a plurality of functional modes, in response to first configuration information. (Ex. A, p. 21, ¶ 67). The interconnection network 110 is also operative to reconfigure a second group of

heterogeneous computational elements to form a second functional unit for a second functional mode of the plurality of functional modes, in response to second configuration information. (Ex. A, p. 21, ¶ 67). The first functional mode differs than the second functional mode, and the plurality of functional modes includes linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, memory operations, and bit-level manipulations. (Ex. A, p. 16, ¶ 49). If the second functional mode is not currently used, one or more of the second group of heterogeneous computational units are reconfigurable to implement the first functional mode. (Ex. A, p. 22, ¶ 71, Fig. 11).

Claim 21 generally relates to a method for allocating hardware resources within an adaptive computing integrated circuit 100. (Ex. A, p. 7, ¶ 29, Figs. 1, 3 and 4). In response to first configuration information, a first group of heterogeneous computational elements is configured to form a first functional unit to implement a first function. (Ex. A, p. 21, ¶ 67). A second group of heterogeneous computational elements is configured to form a second functional unit to implement a second function. (Ex. A, p. 21, ¶ 67). In response to the second configuration information, one or more of the second group of heterogeneous computational elements are reconfigured to implement the first function. (Ex. A, p. 22, ¶ 71, Fig. 11).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1) Whether claims 21 and 23-25 were improperly rejected as anticipated under 35 U.S.C. § 102(b) over U.S. Patent No. 6,046,603 ("New (1)" attached as Exhibit D) which incorporates U.S. Patent No. 6,091,263 ("New (2)" attached as Exhibit E) by reference.

2) Whether claims 1-20 and 22 were improperly rejected as anticipated under 35 U.S.C. § 103(a) over New (1) in view of Wirthlin et al., "A Dynamic Instruction Set Computer," No. 8186-7086-X195 I.E.E.E. 1995 ("Wirthlin" attached as Exhibit F).

The Final Office Action maintained a provisional obviousness-type double patenting rejection based on then co-pending Application No. 10/015,544. (Ex. B, pp. 2-3). Applicant is not appealing the provisional double patenting rejection and will submit a suitable terminal disclaimer, if necessary, should the other objections be overcome.[1]

With regard to claim 21, the Final Office Action cited Col. 5, ll. 39-46 and Fig. 1 of New (1) for "configuring a first group of heterogeneous computational elements and Col. 1, ll. 13-20 and Col. 3, ll. 25-42 to form a first functional unit to implement a first function." (Ex. B, p. 4, ¶ 10(a)). The Final Office Action also cited the same sections in New (1) and New (2) for "configuring a second group of heterogeneous computational elements ... to form a second functional unit to implement a second function." (Ex. B, p. 4, ¶ 10(a)). The Final Office Action asserted that "any rectangular group of computational elements can be partially reconfigured to implement any function, or act as any functional unit the reconfiguration information requires, including groups of computation elements that are grouped together as functional units" citing Col. 1, ll. 56-60 and Col. 5, ll. 39-46 of New (1). (Ex. B, p. 4, ¶ 10(a)). The Final Office Action

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[1] Co-pending Application 10/015,544 has since been abandoned and therefore Applicant believes that a terminal disclaimer is no longer necessary.

cited Col. 5, l. 39 to Col. 6, l. 51 of New (1) for disclosing the feature of reconfiguring the second group of heterogeneous computational elements to implement the first function. (Ex. B, pp. 4-5, ¶ 10(b)).

With regard to claim 1, the Final Office Action cited elements 1A-24A and 1B-24B of Fig. 1 of New (1) as disclosing "a plurality of heterogeneous computational elements." (Ex. B, p. 7, ¶ 16(a)). Fig. 1 and Col. 5, l. 39 - Col. 6, l. 51 of New were cited as disclosing an interconnection network operative to configure the plurality of heterogeneous computational elements. (Ex. B, pp. 4-5, ¶ 16(b)). The Final Office Action cited Col. 5, ll. 39-46 and CLBs 9-16 of Fig. 1 of New (1) and Col. 1, ll. 13-20 and Col. 3, ll. 25-42 of New (2) for "a first group of heterogeneous computational elements" configurable to form a first functional unit to implement a first function. (Ex. B, p. 7, ¶ 16(c)). The Final Office Action also cited CLBs 1-9 of Fig. 1 of New (1) and the same sections in New (1) and New (2) for "a second group of heterogeneous computational elements … configurable to form a second functional unit to implement a second function." (Ex. B, p. 7, ¶ 16(d)). The Final Office Action cited Col. 5, l. 39 to Col. 6, l. 51 of New(1) for reconfiguring the second group of heterogeneous computational elements to implement the first function. (Ex. B, p. 7, ¶ 16(e)). The Final Office Action asserted that "any rectangular group of computational elements can be partially reconfigured to implement any function, or act as any functional unit the reconfiguration information requires, including groups of computation elements that are grouped together as functional units" citing Col. 1, ll. 56-60 and Col. 5, ll. 39-46 of New (1). (Ex. B, p. 7, ¶ 16(e)). The Final Office Action conceded that "New has not explicitly taught wherein if the function is not currently used, one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement the first function." (Ex. B, p. 8, ¶ 17). The Final Office Action indicated

that section 2.2 of Wirthlin teaches the reconfiguring of groups of computational elements (instruction modules) so as to replace idle instruction modules at run-time, thus improving the partial re-configuration speed and overall throughput of the system." (Ex. B, p. 8, ¶ 18).

With regard to claim 6, the Final Office Action indicates that New teaches a plurality of reconfigurable matrices citing elements 601L and 601R of Fig. 1 and Col. 6, ll. 5-10 of New (2). (Ex. B, p. 10, ¶ 23(a)). The Final Office Action cited Col. 1, ll. 56-60 and Col. 5, ll. 39-46 of New (1) for disclosing heterogeneous computational units. (Ex. B, p. 10 ¶ 23(a)). The Final Office Action cites elements 1A-24A and 1B-24B as a plurality of fixed computational elements of each heterogeneous computational unit with distinct first and second architectures. (Ex. B, p. 10, ¶ 23(a)). The Final Office Action indicated that New (1) disclosed a first computational element having the first architecture (elements 1A-24A, Fig. 1) and a second computational element having the second architecture (elements 1B-24B, Fig. 1). (Ex. B, p. 10, ¶ 23(a)). The Final Office Action argued that Col. 3, ll. 41-60 of New (1) discloses the first architecture being distinct from the second architecture. (Ex. B, p. 10, ¶ 23(a)). The Final Office Action asserted New (1) discloses an interconnection network coupled to the heterogeneous computational units. (Ex. B, p. 10, ¶ 23(a)).

The Final Office Action conceded that "New has not explicitly taught wherein if the second operating mode is not currently used, one or more of the second group of heterogeneous computational units are reconfigurable to implement the first operating mode." (Ex. B, p. 12, ¶ 24). The Final Office Action has indicated that Wirthlin teaches the reconfiguring of groups of computational units in the form of instruction modules to replace idle computation units at run time. (Ex. B, p. 12, ¶ 25). The Final Office Action asserts that since New teaches a method of partial reconfiguration of groups of computational units (citing Col. 1, ll. 56-60 and Col. 5, ll. 39-

46 of New (1)), one of ordinary skill in the art would have found it obvious to modify the adaptive computing integrated circuit of New to reconfigure idle groups of computational units. (Ex. B, p. 12, ¶ 25)

With regard to claim 11, the Final Office Action cites elements 1A-24A and 1B-24B and Col. 3, ll. 41-60 of New (1) as disclosing a plurality of heterogeneous computational elements with distinct first and second architectures. (Ex. B, pp. 14-15, ¶ 30(a)). The Final Office Action asserts that the plurality of fixed architecture includes different functions by reasoning that the first computational elements (1A-24A) provide control functions to enable/disable reconfiguration circuitry, and the second computational elements (1B-24B) provide configuration and reconfiguration functions to the circuit. (Ex. B, p. 15, ¶ 30(a)). The Final Office Action cited Fig. 1 and Col. 5, l. 39 to Col. 6, l. 51 of New (1) as disclosing an interconnection network operative to configure the plurality of heterogeneous computational elements. (Ex. B, p. 15, ¶ 30(b)).

The Final Office Action cited Col. 5, ll. 39-46 and CLBs 9-16 of Fig. 1 of New (1) and Col. 1, ll. 13-20 and Col. 3, ll. 25-42 of New (2) for "a first group of heterogeneous computational elements" configurable to form a first functional unit to implement a first function. (Ex. B, p. 15, ¶ 30(c)). The Final Office Action also cited CLBs 1-8 of Fig. 1 of New (1) and the same sections in New (1) and New (2) for "a second group of heterogeneous computational elements … configurable to form a second functional unit to implement a second function." (Ex. B, p. 15, ¶ 30(d)). The Final Office Action cited Col. 5, l. 39 to Col. 6, l. 51 of New(1) for reconfiguring the second group of heterogeneous computational elements to implement the first function. (Ex. B, pp. 15-16, ¶ 30(e)).

The Final Office Action conceded that "New has not explicitly taught wherein if the second function is not currently used, one or more of the second group of heterogeneous computational units are reconfigurable to implement the first function." (Ex. B, p. 16, ¶ 31). The Final Office Action has indicated that Wirthlin teaches the reconfiguring of groups of computational elements in the form of instruction modules to replace idle computation modules at run-time. (Ex. B, p. 16, ¶ 32). The Final Office Action asserts that since New teaches a method of partial reconfiguration of groups of computational elements, "one of ordinary skill in the art would have found it obvious to modify the adaptive computing integrated circuit of New to reconfigure idle groups of computational elements." (Ex. B, p. 16, ¶ 32).

With regard to claim 16, the Final Office Action cites elements 1A-24A and 1B-24B and Col. 3, ll. 41-60 of New (1) as disclosing a plurality of heterogeneous computational elements with distinct first and second architectures. (Ex. B, pp. 18-19, ¶ 37(a)). The Final Office Action asserts that Fig. 1 and Col. 1, ll. 56-60 and Col. 5, ll. 39-46 of New (1) discloses an interconnection network coupled to the plurality of heterogeneous computational elements for configuration of the computational elements. (Ex. B, p. 19, ¶ 37(b)).

The Final Office Action conceded that "New has not explicitly taught wherein if the second functional mode is not currently used, one or more of the second group of heterogeneous computational units are reconfigurable to implement the first functional mode." (Ex. B, p. 20, ¶ 38). The Final Office Action has indicated that Wirthlin teaches the reconfiguring of groups of computation units in the form of instruction modules to replace idle computation units at run time. (Ex. B, pp. 20-21, ¶ 39). The Final Office Action asserts that since New teaches a method of partial reconfiguration of groups of computational units, "one of ordinary skill in the art would

have found it obvious to modify the adaptive computing integrated circuit of New to reconfigure idle groups of computational units." (Ex. B, p. 21, ¶ 39).

VII. ARGUMENT

For the Board's convenience, claims 21 and 23-25 are one group that will stand or fall together with regard to the anticipation rejection. Claims 1-20 and 22 are one group that will stand or fall by themselves with regard to the obviousness rejection.

A. CLAIMS 21 AND 23-25 ARE IMPROPERLY REJECTED UNDER 35 U.S.C. 102 BASED ON NEW BECAUSE NEW DOES NOT DISCLOSE HETEROGENEOUS COMPUTATIONAL ELEMENTS

The Examiner has failed to discharge his burden in establishing a *prima facie* case of anticipation with regard to New (1) in relation to claims 21 and 23-25. These claims all require using an interconnection network to transfer adaptation information to configure the heterogeneous computational elements in the adaptable integrated circuit to perform different functions.

1. The Significant Differences Between Prior Art Homogeneous Computational Elements And The Heterogeneous Computational Elements Of Claims 21 And 23-25.

New (1) does not disclose using the interconnection network to configure heterogeneous computation elements. New (1) relates to a prior art field programmable gate array (FPGA) which is a commonly known array of homogeneous computational elements that suffer from many disadvantages. (Exhibit G, definition of FPGA from Electronics Information On-Line). Fig. 1 of New (1) shows an array of identical configurable logic blocks (CLBs) which may be selected as a rectangular set for configuration of different functions. (Ex. D, Col. 5, ll. 39-46). The CLBs 1-24 all include an enabling circuit (e.g., NAND gate 1A) to disable or enable an associated reconfiguration circuit (e.g., 1B). (Ex. D, Col. 3, ll. 46-50). The NAND gates in Fig. 1 of New (1) are simply switches, they do not compute anything. The CLBs as described in Col. 5, ll. 54-61 of New (2) are identical Xilinx XC4000EX FPGAs. (Ex. E, Figs. 2-5).

Homogeneous computational elements such as the CLBs in New require more integrated circuit area, time and power than the heterogeneous computational elements in the claims. (Ex. A, pp. 2-3, ¶ 7). In order to configure such homogeneous gates, an extensive interconnect network must be used, resulting in high capacitance causing slow operation and high power consumption. (Ex. A, pp. 2-3, ¶ 7). Further such FPGAs are subject to chaotic routing thus resulting in delay and wasted logic resources. (Ex. A, pp. 2-3, ¶ 7). In fact, the specification explains:

> The third and perhaps most significant concept of the present invention, and a marked departure from the concepts and precepts of the prior art, is the concept of reconfigurable "heterogeneity" utilized to implement the various selected algorithms mentioned above. As indicated above, prior art reconfigurability has relied exclusively on homogeneous FPGAs, in which identical blocks of logic gates are repeated as an array within a rich, programmable interconnect, with the interconnect subsequently configured to provide connections between and among the identical gates to implement a particular function, albeit inefficiently and often with routing and combinatorial problems.

(Ex. A, p. 11, ¶ 39). This section of the specification clearly differentiates the present invention from homogeneous FPGA art such as New (1).

2. New (1) Does Not Disclose Heterogeneous Computational Elements As All Of The CLB Computational Elements That Are Reconfigured Are Identical

The Final Office Action cites elements 9-16 of Fig. 1 and Col. 5, ll. 39-46 of New (1) for a first group of heterogeneous computational elements that are configured and elements 1-8 of Fig. 1 as a second group of heterogeneous computational elements. (Ex. B, p. 4, ¶10(a)). However as explained above, those elements are all identical CLBs. Col. 5, ll. 39-45 confirms that New (1) relates to a prior art FPGA with homogeneous computational elements such as FPGA 100 which selects certain elements for the configuration. The selected elements in New are all identical, leading to the problems with homogeneous computational elements described in the present specification.

Claims 21 and 23-25 are therefore allowable over New (1) since New (1) does not disclose first and second groups of heterogeneous computational elements that are configured and reconfigured. These claims require that the computational elements are different because they are heterogeneous. As explained above, the computational elements in Fig. 1 of New (1) which are parts of the first and second groups (elements 9-16 and elements 1-8) are identical and therefore cannot be heterogeneous. The Final Office Action has read first and second heterogeneous elements to means that the two elements are different because one group in New (1) is reconfigured while another group remains static. (Ex. B, p. 25, ¶ 51). This is simply erroneous as the CLB computational elements in both groups are identical. Even accepting the Examiner's argument, the CLB computational elements in New (1) are exactly the same prior to configuration or reconfiguration, they only differ after configuration. Since the computational elements in claim 21 are different prior to configuration and reconfiguration (e.g., "configuring a first group of heterogeneous elements"), New (1) does not anticipate these features because its CLBs are identical prior to (and after for that matter) configuration.

3. The Final Office Action Errs In Attempting To Broaden The Term "Heterogeneous Computational Elements" To Include Any Programmable Device

The Final Office Action has asserted that heterogeneous computational elements "simply need to be different." (Ex. B, p. 24, ¶ 50). The Final Office Action continues by reasoning "whether the difference is in function or structure, it does not matter, since the claim has not specified the differences between the computation elements are, e.g. how the computation elements are different." (Ex. B, p. 24, ¶ 50). The Final Office Action rejects the argument made by Applicant that the CLBs in New (1) are homogeneous because each has the same physical structure by asserting that "the sections of the specification referred to in the arguments do not

contain an explicit and precise definition regarding the meaning of heterogeneous means different structure." (Ex. B, p. 24, ¶ 50). The Final Office Action further asserts that any limitations in the specification that define heterogeneous computational elements should not be read into the claim elements. (Ex. B, p. 25, ¶ 51).

The Final Office Action takes an unreasonable reading of the claim scope given the specification, claim language and commonly understood meaning of FPGAs. (e.g., Ex. G). First, the prior art FPGAs in New (1) are clearly different from the heterogeneous computational elements as explained above. (e.g., Ex. A, pp. 2-3 ¶ 7 and p. 11, ¶ 39). Specifically:

> The third and perhaps most significant concept of the present invention, and a marked departure from the concepts and precepts of the prior art, is the concept of reconfigurable "heterogeneity" utilized to implement the various selected algorithms mentioned above. As indicated above, prior art reconfigurability has relied exclusively on homogeneous FPGAs, in which identical blocks of logic gates are repeated as an array within a rich, programmable interconnect, with the interconnect subsequently configured to provide connections between and among the identical gates to implement a particular function, albeit inefficiently and often with routing and combinatorial problems.

(Ex. A, p. 11, ¶ 39). Although limitations in the specification are not to be read into the claims, the specification serves as the patentee's lexicography and thus the definition of heterogeneous computational elements should be afforded the meaning of the patentee through the specification, especially when consistent with commonly understood definitions of the terms. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1303, 1316 (Fed. Cir. 2005). The Final Office Action's citation of *In re Van Geuns*, 988 F.2d 1181 (Fed. Cir. 1993) is inapplicable as in that case the term "uniform magnetic field" was not expressly limited to NMR and MRI apparatus in the claim at issue. *Id.* at 1184-85. In contrast, the term "heterogeneous" is an express limitation in the claims in this case and the specification clearly differentiates heterogeneous computational elements from homogeneous logic such as the FPGA disclosed in New (1). Applicant respectfully submits that the plain meaning of heterogeneous computational elements read in

context of the specification are sufficient to distinguish the homogeneous CLBs in New cited by the Final Office Action.

Second, the interpretation of heterogeneous computational elements offered by the Final Office Action renders the well known prior art homogeneous FPGAs meaningless. If identical physical hardware units are considered heterogeneous because of their inherent function of being configured and reconfigured, there can be no homogeneous elements. This flies in the face of the known prior art as well as the specification.

Third, the interpretation taken by the Final Office Action is inconsistent with the other elements of the claim. Claim 21 requires the computational elements to be heterogeneous prior to receiving configuration information to be configured. In contrast, New (1) discloses identical computational elements prior to receiving configuration or reconfiguration information. It is clear that the computational elements in New (1) cited by the Final Office Action are do not fall under the meaning of the heterogeneous computational elements in the claims and therefore claims 21 and 23-25 are allowable over New (1).

B. CLAIMS 1-20 AND 22 ARE IMPROPERLY REJECTED UNDER 35 U.S.C. 103 BASED ON NEW AND WIRTHLIN BECAUSE NEITHER OF THE REFERENCES DISCLOSE HETEROGENEOUS COMPUTATIONAL UNITS OR ELEMENTS

The Examiner has failed to discharge his burden in establishing a *prima facie* case of anticipation in relation to claims 1-20 and 22. All of these claims include the feature of a plurality of heterogeneous computational units or elements. In addition, claims 6, 11 and 16 specifically require that the computational elements have two different fixed architectures. As such, New (1) does not include such features as New (1) is based on an FPGA which is by definition an array of homogeneous computing elements. Wirthlin also does not disclose

heterogeneous computing elements. Wirthlin relates generally to a Dynamic Interaction Set Computer (DISC) implemented with partially reconfigurable FPGAs with homogeneous computing elements (Ex. F, p. 99, Abstract). The combination of New (1) and Wirthlin therefore would only result in a computing engine based on groups of core homogeneous computing elements and would not anticipate the heterogeneous computational elements in these claims for the reasons detailed above in Section A.

1. Claims 1, 11 and 16 Require Heterogeneous Computing Elements And Are Not Obvious Over The Combination Of New and Wirthlin

With regard to claims 1, 11 and 16 the Final Office Action cited elements 1A-24A and 1B-24B of Fig. 1 of New (1) as disclosing "a plurality of heterogeneous computational elements." (Ex. B, p. 7, ¶ 16(a), p. 14, ¶ 30(a), p. 18, ¶ 37(a)). The Final Office Action cited Col. 5, ll. 39-46 and Fig. 1 of New (1) for configuring a first group of heterogeneous computational elements and Col. 1, ll. 13-20 and Col. 3, ll. 25-42 of New (2) as disclosing forming a first functional unit to implement a first function. (Ex. B, p. 7, ¶ 16(c), p. 14, ¶ 30(c), p. 18, ¶ 37(b)). The Final Office Action also cited the same sections in New (1) and New (2) for "configuring a second group of heterogeneous computational elements ... to form a second functional unit to implement a second function." (Ex. B, p. 7, ¶ 16(d), p. 14, ¶ 30(d), p. 18, ¶ 37(b)). The Final Office Action erroneously asserts that CLBs 1-24 are heterogeneous because they are configured for different functions. The Final Office Action asserts that section 2.2 of Wirthlin teaches the reconfiguring of groups of computational elements (instruction modules) so as to replace idle instruction modules at run-time, thus improving the partial re-configuration speed and overall throughput of the system. (Ex. B, p. 8, ¶ 17, p. 16, ¶ 31, pp. 20-21, ¶ 39). As explained above, the CLBs 1-24 in New (1) and the modules of the FPGA in Wirthlin are exactly the same hardware structure and are therefore homogeneous both before and after configuration.

Both New and Wirthlin are descriptive of prior art homogeneous computational elements and thus the combination of these references do not render claims 1, 11 and 16 obvious.

2. Claims 6, 11 and 16 Are Not Obvious Over The Combination Of New and Wirthlin Because None Of The References Disclose Nor Suggest Computational Elements with Different Fixed Architectures

Claims 6, 11 and 16 also require that the "plurality of fixed computational elements including a first computational element having a first architecture and a second computational element having a second architecture, the first architecture distinct from the second architecture." The Final Office Action has cited elements 1A-24A and 1B-24B against these elements. (Ex. B, p. 10, ¶ 23(a), pp. 14-15, ¶ 30(a), pp.18-19, ¶ 37(a)). These elements are all components of the CLBs 1-24 which each include identical reconfiguration circuits (1A-24A) and selection circuits (NAND gates 1B-24B). (Ex. D, Col. 3, ll. 42-45). Contrary to the Final Office Action' assertion, the selection circuits are merely NAND gates and are not a computational element. The only computational capabilities are with the reconfiguration circuits 1A-24A, which are all identical. Thus, the CLBs 1-24 in New (1) have only one fixed architecture, namely the selection circuit (e.g., 1B) in combination with the reconfiguration circuit (e.g., 1A). The computational elements thus do not includes a first fixed architecture and a second different fixed architecture. There is no distinction between the architectures for any of the CLBs and therefore New (1) does not disclose or suggest computational elements having a "first architecture distinct from the second architecture." Both New and Wirthlin are descriptive of prior art homogeneous computational elements with identical fixed architectures and thus the combination of these references do not render claims 6, 11 and 16 obvious.

VIII. CLAIMS APPENDIX

A clean copy of the claims 1-25 involved in the appeal is included in the Claims Appendix.

IX. EVIDENCE APPENDIX

A copy of the evidence relied upon by the appellant is included in the Evidence Appendix and is herein referenced. A list of evidence and where each was entered in the record is included in the Index to the Appendices.

X. RELATED PROCEEDINGS APPENDIX

As there are no related proceedings, no information is provided in the Related Proceedings Appendix.

XI. CONCLUSION

For at least the foregoing reasons, the final rejection of appealed claims 1-25 set forth in the Final Office Action mailed December 9, 2005, should be reversed.

Respectfully submitted,

Date: December 20, 2007

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APPENDICES

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CLAIM APPENDIX

CLAIMS APPENDIX
CLEAN COPY OF CLAIMS ON APPEAL

1. An adaptive computing integrated circuit configurable to perform a plurality of functions, comprising:

a plurality of heterogeneous computational elements; and

an interconnection network coupled to the plurality of heterogeneous computational elements, the interconnection network operative to configure the plurality of heterogeneous computational elements;

wherein a first group of heterogeneous computational elements is configurable to form a first functional unit to implement a first function;

wherein a second group of heterogeneous computational elements is configurable to form a second functional unit to implement a second function; and

wherein if the second function is not currently used, one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement the first function.

2. The adaptive computing integrated circuit of claim 1 wherein if the second function is not currently used, the one or more of the second group of heterogeneous computational elements are reconfigurable to implement the first function by forming one or more additional instances of the first functional unit.

3. The adaptive computing integrated circuit of claim 1 wherein if the second function is not currently used, one or more of the first group of heterogeneous computational elements and the one or more of the second group of heterogeneous computational elements are reconfigurable to form a single functional unit to implement the first function.

4. The adaptive computing integrated circuit of claim 1 wherein if the second function is not currently used, the one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement one or more of the plurality of functions other than the second function.

5. The adaptive computing integrated circuit of claim 1 wherein if a third function is to be implemented, one or more of the first group of heterogeneous computational elements and/or the one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement the third function.

6. An adaptive computing integrated circuit, comprising:

a plurality of reconfigurable matrices, the plurality of reconfigurable matrices including a plurality of heterogeneous computational units, each heterogeneous computational unit having a plurality of fixed computational elements, the plurality of fixed computational elements including a first computational element having a first architecture and a second computational element having a second architecture, the first architecture distinct from the second architecture, the plurality of heterogeneous computational units coupled to an interconnect network and reconfigurable in response to configuration information; and

a matrix interconnection network coupled to the plurality of reconfigurable matrices, the matrix interconnection network operative to reconfigure the plurality of reconfigurable matrices in response to the configuration information for a plurality of operating modes;

wherein a first group of heterogeneous computational units is reconfigurable to form a first functional unit to implement a first operating mode;

wherein a second group of heterogeneous computational units is reconfigurable to form a second functional unit to implement a second operating mode;

wherein if the second operating mode is not currently used, one or more of the second group of heterogeneous computational units are reconfigurable to implement the first operating mode.

7. The adaptive computing integrated circuit of claim 6 wherein if the second operating mode is not currently used, the one or more of the second group of heterogeneous computational units are reconfigurable to implement the first operating mode by forming one or more additional instances of the first functional unit.

8. The adaptive computing integrated circuit of claim 6 wherein if the second operating mode is not currently used, one or more of the first group of heterogeneous computational units and the one or more of the second group of heterogeneous computational units are reconfigurable to form a single functional unit to implement the first operating mode.

9. The adaptive computing integrated circuit of claim 6 wherein if the second operating mode is not currently used, the one or more of the second group of heterogeneous computational units are reconfigurable to implement one or more of the plurality of operating modes other than the second operating mode.

10. The adaptive computing integrated circuit of claim 6 wherein if a third operating mode is to be implemented, one or more of the first group of heterogeneous computational units and/or

the one or more of the second group of heterogeneous computational units are reconfigurable to implement the third operating mode.

11. An adaptive computing integrated circuit, comprising:

a plurality of heterogeneous computational elements, the plurality of heterogeneous computational elements including a first computational element and a second computational element, the first computational element having a first fixed architecture of a plurality of fixed architectures and the second computational element having a second fixed architecture of the plurality of fixed architectures, the first fixed architecture being different than the second fixed architecture, and the plurality of fixed architectures including functions for memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability; and

an interconnection network coupled to the plurality of heterogeneous computational elements, the interconnection network operative to configure the plurality of heterogeneous computational elements;

wherein a first group of heterogeneous computational elements is reconfigurable to form a first functional unit to implement a first function;

wherein a second group of heterogeneous computational elements is reconfigurable to form a second functional unit to implement a second function; and

wherein if the second function is not currently used, one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement the first function.

12. The adaptive computing integrated circuit of claim 11 wherein if the second function is not currently used, the one or more of the second group of heterogeneous computational elements are reconfigurable to implement the first function by forming one or more additional instances of the first functional unit.

13. The adaptive computing integrated circuit of claim 11 wherein if the second function is not currently used, one or more of the first group of heterogeneous computational element and the one or more of the second group of heterogeneous computational elements are reconfigurable to form a single functional unit to implement the first function.

14. The adaptive computing integrated circuit of claim 11 wherein if the second function is not currently used, the one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement on or more of the plurality of functions other than the second function.

15. The adaptive computing integrated circuit of claim 11 wherein if a third function is to be implemented, one or more of the first group of heterogeneous computational elements and/or the one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement the third function.

16. An adaptive computing integrated circuit, comprising:

a plurality of heterogeneous computational elements, the plurality of heterogeneous computational elements including a first computational element and a second computational element, the first computational element having a first fixed architecture and the second

computational element having a second fixed architecture, the first fixed architecture being different than the second fixed architecture; and

an interconnection network coupled to the plurality of heterogeneous computational elements, the interconnection network operative to configure a first group of heterogeneous computational elements to form a first functional unit for a first functional mode of a plurality of functional modes, in response to first configuration information, and the interconnection network further operative to reconfigure a second group of heterogeneous computational elements to form a second functional unit for a second functional mode of the plurality of functional modes, in response to second configuration information, the first functional mode being different than the second functional mode, and the plurality of functional modes including linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, memory operations, and bit-level manipulations;

wherein if the second functional mode is not currently used, one or more of the second group of heterogeneous computational units are reconfigurable to implement the first functional mode.

17. The adaptive computing integrated circuit of claim 16 wherein if the second functional mode is not currently used, the one or more of the second group of heterogeneous computational elements are reconfigurable to implement the first functional mode by forming one or more additional instances of the first functional unit.

18. The adaptive computing integrated circuit of claim 16 wherein if the second functional mode is not currently used, one or more of the first group of heterogeneous computational

elements and the one or more of the second group of heterogeneous computational elements are reconfigurable to form a single functional unit to implement the first functional mode.

19. The adaptive computing integrated circuit of claim 16 wherein if the second functional mode is not currently used, the one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement one or more of the plurality of functional modes other than the second functional mode.

20. The adaptive computing integrated circuit of claim 16 wherein if a third functional mode is to be implemented, one or more of the first group of heterogeneous computational elements and/or the one or more of the second group of heterogeneous computational elements are reconfigurable by the interconnection network to implement the third functional mode.

21. A method for allocating hardware resources within an adaptive computing integrated circuit, comprising:

in response to first configuration information, configuring a first group of heterogeneous computational elements to form a first functional unit to implement a first function and configuring a second group of heterogeneous computational elements to form a second functional unit to implement a second function; and

in response to second configuration information, reconfiguring one or more of the second group of heterogeneous computational elements to implement the first function.

22. The method of claim 21 wherein the second configuration information is generated when the second function is not currently used.

23. The method of claim 21 wherein in response to the second configuration information, the one or more of the second group of heterogeneous computational elements are reconfigured to form one or more additional instances of the first functional unit to implement the first function.

24. The method of claim 21 wherein in response to the second configuration information, one or more of the first group of heterogeneous computational elements and the one or more of the second group of heterogeneous computational elements are reconfigured to form a single functional unit to implement the first function.

25. The method of claim 21 further comprising:

in response to third configuration information, reconfiguring one or more of the first group of heterogeneous computational elements and/or the one or more of the second group of heterogeneous computational elements to implement a third function.

EVIDENCE APPENDIX